

REMARKS

Claims 1-16 are pending in the application. Claims 1-4, 8 and 14 have been amended and Replacement Sheets for **Fig. 1**, **Fig. 3** and **Fig. 4** have been added by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, the drawings were objected to because the details cannot be read in **Fig. 1** and **Fig. 3**; claim 1 is rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement; claims 1-16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention; and claims 1-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over “A Custom VLSI Architecture for the Solution of FDTD Equations” (Placidi) in view of U.S. Patent No. 5,951,627 (Kiamilev et al).

Amendments to the Specification

The specification has been amended to clarify the invention. In particular, the specification has been amended to correct a typographical error in not including reference number **20** in the drawing of **Fig. 1**. Support for the amendments is provided in the paragraph beginning at page 5, line 24; and shown at least in **Fig. 1** at reference number **20**. Therefore, it is respectfully submitted that the amendments raise no questions of new matter.

Amendments to the Drawings

The drawings were objected to because the details in **Fig. 1** and **Fig. 3** cannot be read. Replacements Sheets are submitted herewith to clarify the invention by providing legible versions of **Fig. 1** and **Fig. 3**. Support for the Replacement Sheets is provided at least by the original **Fig. 1** and **Fig. 3**. Therefore, it is respectfully submitted that **Fig. 1** and **Fig. 3** are now legible and that the outstanding drawing objection is moot and should be withdrawn.

35 U.S.C. § 112 Rejections

Claim 1 was rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Reconsideration is respectfully requested.

As discussed above, the specification and the drawings have been amended to clarify the invention. In addition, claim 1 has been amended to recite:

[a] method for organizing cache memory for hardware acceleration of the FDTD method in a ~~very high bandwidth, dual-port on-chip memory, comprising:~~
creating a plurality of small banks of internal memory; and
~~arranging routing data from the plurality of small banks of internal memory to computation engines so that all data dependencies of the computational engines are satisfied when each read address is presented to the plurality of small banks of internal memory capable of being statically wired.~~

Support for the amendment is provided at least at page 5, line 23 to page 6, line 8; and shown at least in **Fig. 1**, reference **24** of the specification. Therefore, it is respectfully submitted that these amendments clarify how to make and use the invention and thus, it is requested that the outstanding rejection be withdrawn.

Claims 1-16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Reconsideration is respectfully requested.

Claims 1, 2, 8 and 14 have been amended to clarify the invention. In particular, the claims have been amended to provide proper antecedent basis for the phrase “FDTD method” and to remove the phrase “very high bandwidth.” Therefore, it is respectfully submitted that the outstanding rejections are moot and should be withdrawn.

35 U.S.C. § 103 Rejections

Claims 1-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Placidi in view of Kiamilev et al. Reconsideration is respectfully requested.

Claims 1-4, 8 and 16 have been amended to clarify the invention. In particular, claim 1 has been amended to recite:

arranging routing data from the plurality of small banks of internal memory to computation engines so that all data dependencies of the computational engines are satisfied when each read address is presented to the plurality of small banks of internal memory capable of being statically wired.

Similarly, claim 2 and claim 8 have been amended to recite:

wherein said connecting steps route data, dependent on direction, from said memory banks to the corresponding computation engines when each read address is presented to said memory banks.

Moreover, claim 14 has been amended to recite:

wherein the organization scheme further comprises a first plurality of dual-port input memory banks connected to corresponding one-cycle delay elements, a plurality of computation engines connected to corresponding delay elements, a second plurality of input memory banks connected to corresponding computation engines, and a plurality of output memory banks connected to corresponding computation engines.

Support for the amendments is provided at least at page 5, line 23 to page 6, line 8; and at least in original claims 3-6; and shown at least in **Fig. 1**, reference **24** of the specification. Therefore, it is respectfully submitted that these amendments raise no questions of new matter.

Placidi discloses a digital system dedicated to the fast execution of the FDTD algorithm used for electromagnetic simulation.¹ In particular, Placidi discloses an architecture that includes a dedicated floating-point unit (FPU), some register banks, a PCI Target Interface Circuit, a set of control units (CU) and several *external* SDRAM memories (emphasis added).² Further, Placidi discloses five 32 bit data busses to allow parallel data fetching and that all data required to update the field components from the on-board SDRAM are obtained in *just two read*

¹ Placidi at ABSTRACT.

² *Id.* at Fig. 2; pg. 574, Section 3, first paragraph.

operations (emphasis added).³ Further, Placidi discloses use of additional registers for temporary data storage due to sequential data fetch.⁴

Further, Placidi discloses the fully-pipelined floating-point unit (FPU) based on IEEE-754 standard floating point representation includes internal delay elements **d**.⁵ Furthermore, Placidi discloses the on-chip CU that takes care of data flow between the SDRAM and the FPU.⁶ Moreover, Placidi discloses that by issuing proper instructions to the memory and the datapath, subsequent operations needed by the FDTD algorithm (e.g., loading of the constant coefficients, initialization of the system variables, acquisition of the field external stimuli, actual field-component update, write-back of the results to the system) can be executed.⁷

However, Placidi nowhere discloses, as claims 2 and 8 recite:

wherein said connecting steps route data, dependent on direction, from said memory banks to the corresponding computation engines when *each read address is presented* to said memory banks. (emphasis added).

That is, in contrast to Placidi, which requires two read operation, the claimed invention provides the required data on each read cycle. In addition, claim 1 uses similar language to claims 2 and 8 and thus Placidi does not disclose all of the limitations of claim 1 for the same reasons as discussed for claim 8. Further, Placidi does not disclose all of the connecting of elements of claim 14 as recited above. Therefore, it is respectfully submitted that Placidi does not disclose the claimed invention.

The outstanding Office Action acknowledges other deficiencies in Placidi and attempts to correct these deficiencies with Kiamilev et al. However, Kiamilev et al. cannot correct all of the deficiencies of Placidi as will be discussed below.

Kiamilev et al. discloses a high-performance photonic chipset for computing 1-D complex fast Fourier transform (FFT) calculations.⁸ In particular, Kiamilev et al. discloses dual-

³ *Id.* at Section 3, second paragraph.

⁴ *Id.* at Section 3, third paragraph.

⁵ *Id.* at FIG. 3; Section 3, fifth paragraph.

⁶ *Id.* at FIG. 3; Section 3, sixth paragraph.

⁷ *Id.* at FIG. 3; Section 3, sixth paragraph.

⁸ Kiamilev et al. at ABSTRACT.

port memory is used to permit simultaneous read-write access to adjacent addresses in the data banks needed by each stage.⁹

However, Kiamilev et al. nowhere discloses, as claims 2 and 8 recite:

wherein said connecting steps route data, dependent on direction, from said memory banks to the corresponding computation engines when *each read address is presented* to said memory banks. (emphasis added).

That is, in contrast to Kiamilev et al., nowhere discloses providing the required data on each read cycle. In addition, claim 1 uses similar language to claims 2 and 8 and thus, Kiamilev et al. does not disclose all of the limitations of claim 1 for the same reasons as discussed for claim 8. Further, Kiamilev et al. does not disclose all of the connecting of elements of claim 14 as recited above. Thus, it is respectfully submitted that Kiamilev et al. does not overcome all of the deficiencies of Placidi. Therefore, neither Placidi nor Kiamilev et al., whether taken individually or in combination, disclose, suggest or make obvious the claimed invention and thus, claims 1, 2, 8 and 14, and claims dependent thereon patentably distinguish thereover.

⁹ *Id.* at ABSTRACT.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 22-0185, under Order No. 10354-00003-US1 from which the undersigned is authorized to draw.

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529160_1

Respectfully submitted,

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